What is claimed is:

1. An interrupt signal processing apparatus for processing a request for interruption from one device to the other device, connected between the one device and the other device, each being operated on either of a first clock and a second clock, comprising:

an interrupt setting pulse generating section, when receiving an interrupt requesting signal from said one device, generates an interrupt setting pulse signal by using timing provided by said first clock on which said one device is operated;

a register, when receiving said interrupt setting pulse signal, to store said interrupt setting pulse signal as a signal for interruption to said other device;

a first synchronization unit to output said interrupt signal fed from said register to the other device, in synchronization with said second clock on which the other device is operated;

an interrupt clearing pulse generating section, when receiving an interrupt clearing request signal from said other device which has received said interrupt signal through said synchronization section, to output an interrupt clearing pulse signal using timing provided by said second clock in order to reset said register used to store said interrupt signal;

a second synchronization section to output an interrupt permission signal, in synchronization with said first clock, to said one device, when said register has received said clearing pulse signal;

a control circuit provided between said interrupt setting pulse generating section and said interrupt clearing pulse generating section to

control generation, using one pulse out of said interrupt setting pulse signal and said interrupt clearing pulse signal, of the other pulse out of said interrupt setting pulse and said interrupt clearing signal; and

a delay circuit to provide, while said one pulse signal is being input to said register, a time delay to operations of said synchronization section being operated in synchronization with said clock on which said pulse generating section used to generate said other pulse signal is operated, in order to prevent duplicated inputting of said both pulse signals to the register.

2. The interrupt signal processing apparatus according to Claim 1, wherein each of said first and second clocks has a different clock speed.

3. The interrupt signal processing apparatus according to Claim 2, wherein a speed of said clock on which said pulse generating section to generate said one of said pulse signals is operated is lower than that of said clock on which said pulse generating section to generate said other of said pulse signals is operated and wherein said delay circuit provides a time delay being equivalent to a clock period of said low-speed clock to said synchronization section.

4. The interrupt signal processing apparatus according to Claim 2, wherein said register is made up of a flip-flop having a set terminal, a reset terminal and an output terminal in which an output signal is switched between two values by selective inputting of a signal to both terminals and wherein said interrupt setting pulse signal is input to said set terminal and said interrupt clearing pulse is input to said reset terminal and wherein an

output signal from said output terminal is input to said both synchronization sections.

5. The interrupt signal processing apparatus according to Claim 2, wherein said control circuit, while said interrupt setting pulse signal is being input in said register, controls said interrupt clearing pulse generating section in order to stop generation of said interrupt clearing pulse generating section by said interrupt clearing pulse generating section and wherein said delay circuit, while said interrupt setting pulse signal is outputting from the interrupt setting pulse generating section, provides a time delay to the transmission of said interrupt signal fed from said register to said first synchronization section.

6. The interrupt signal processing apparatus according to Claim 2, said control circuit, while said interrupt clearing pulse signal is being input to said register, controls said interrupt setting pulse generating section in order to stop the generation of said interrupt setting pulse signal and wherein said control circuit, while said interrupt clearing pulse signal is outputting from said interrupt clearing pulse generating section, provides a time delay to the transmission of an interrupt permission signal fed from said register to said second synchronization section.

7. The interrupt signal processing apparatus according to Claim 5, wherein said delay circuit is made up of a D flip-flop having a clock input terminal, data input terminal and output terminal and wherein said first clock is input to said clock input terminal and said interrupt permission

signal fed from said register to said second synchronization section is input and said interrupt permission signal is output to said output terminal in synchronization with operations of said clock terminal.

8. The interrupt signal processing apparatus according to Claim 6, wherein said delay circuit is made up of a D flip-flop having a clock input terminal to which said second clock is input, a data input terminal to which said interrupt signal fed from said register to said first synchronization section is input and an output terminal which outputs said interrupt signal in synchronization with operations of said clock terminal and is made up of an OR circuit to which said interrupt signal fed from said output terminal of said D flip-flop and said interrupt permission signal fed from said register are input and wherein an output from said OR circuit is input to said first synchronization section.

9. The interrupt signal processing apparatus according to Claim 5, wherein said delay circuit is made up of an AND circuit to which an output signal fed from said register and a reversed signal of said interrupt setting pulse are input and wherein an output of said logical circuit is input to said both synchronization sections.

10. The interrupt signal processing apparatus according to Claim 6, wherein said delay circuit is made up of an OR circuit to which an output signal fed from said register and said interrupt clearing pulse are input and wherein an output from said OR circuit is input to said both synchronization sections.

11. The interrupt signal processing apparatus according to Claim 2, wherein said interrupt setting pulse generating section is made up of a D first flip-flop having a data input terminal to which said interrupt requesting signal fed from said one device is input, a clock input terminal to which said first clock is input and an output terminal from which said signal is output with a delay being equivalent to one clock period of said first clock in synchronization with said first clock and of a second D flip-flop having a data input terminal to which said signal is input from said output terminal, a clock input terminal to which said first clock is input and an output terminal from which a reversed signal of said signal with a delay being equivalent to one clock period of said first clock is output in synchronization with said clock terminal and of an OR circuit to which said both signals fed from said output terminals of said first and second D flip-flop are input and wherein said AND circuit outputs, in synchronization with said first clock, one pulse with a pulse width being equivalent to one clock period of said first clock, as the interrupt setting pulse signal to said register.

12. The interrupt signal processing apparatus according to Claim 11, wherein said second D flip-flop has a set input terminal receiving a control signal from said control circuit and outputs, while receiving said control signal, said reversed signal to said output terminal, which causes said interrupt setting pulse generating section, while receiving said control signal from said control circuit, to stop the outputting of said interrupt setting pulse signal.

13. The interrupt signal processing apparatus according to Claim 2, wherein said interrupt clearing pulse generating section is made up of a first D flip-flop having a data input terminal to which said interrupt clearing request signal fed from said other device is input, a clock input terminal to which said second clock is input and an output terminal which outputs said signal with a delay being equivalent to one clock period of said second clock in synchronization with said second clock and of a second D flip-flop having a data input terminal to which said signal fed from said output terminal is input, a clock input terminal to which said second clock is input and an output terminal which outputs a reversed signal of said signal with a delay being equivalent to one clock period of said clock in synchronization with operations of said clock terminal and of an AND circuit to which said both signals fed from said output terminals of said first and second D flip-flop are input, wherein said AND circuit outputs one pulse having a pulse width being equivalent to one clock period of said second clock as said interrupt clearing pulse signal, in synchronization with said second clock, to said register.

14. The interrupt signal processing apparatus according to Claim 13, wherein said second D flip-flop has a set input terminal receiving a control signal from said control circuit and outputs, while receiving said control signal, said reversed signal to said output terminal, which causes said interrupt clearing pulse generating section, while receiving said control signal from said control circuit, to stop the outputting of said interrupt clearing pulse signal.

15. The interrupt signal processing apparatus according to Claim 2, wherein said first synchronization section is provided with a first D flip-flop having a data input terminal to which said interrupt signal is input from said delay circuit, a clock input terminal to which said second clock is input and an output terminal which outputs said signal with a delay being equivalent to one clock period of said second clock in synchronization with said clock and with a second D flip-flop having a data input terminal to which said signal is input from said output terminal, a clock input terminal to which said clock is input and an output terminal which outputs said signal with a delay being equivalent to one clock period of said second clock in synchronization with said second clock, to said other device.

16. The interrupt signal processing apparatus according to Claim 2, wherein said second synchronization section is made up of a first D flip-flop having a data input terminal to which said interrupt permission signal is input from said delay circuit, a clock input terminal to which said first clock is input and an output terminal which outputs said signal with a delay being equivalent to one clock period of said first clock in synchronization with said first clock and of a second D flip-flop having a data input terminal to which said signal is input from said output terminal, a clock input terminal to which said first clock is input and an output terminal which outputs said signal with a delay being equivalent to one clock period of said first clock in synchronization with said first clock, to said one device.

17. An interrupt signal processing apparatus for processing a request for interruption from one device to the other device, connected between the one

device and the other device, each being operated on either of a first clock and a second clock, comprising:

an interrupt setting pulse generating section, when receiving an interrupt requesting signal from said one device, generates an interrupt setting pulse signal by using timing provided by said first clock on which said one device is operated;

a register, when receiving said interrupt setting pulse signal, to store said interrupt setting pulse signal as a signal for interruption to said other device;

a first synchronization unit to output said interrupt signal fed from said register to the other device, in synchronization with said second clock on which the other device is operated;

an interrupt clearing pulse generating section, when receiving an interrupt clearing request signal from said other device which has received said interrupt signal through said synchronization section, to output an interrupt clearing pulse signal using timing provided by said second clock in order to reset said register used to store said interrupt signal;

a second synchronization section to output an interrupt permission signal, in synchronization with said first clock, to said one device, when said register has received said clearing pulse signal;

a control circuit provided between said interrupt setting pulse generating section and said interrupt clearing pulse generating section to control generation, using one pulse out of said interrupt setting pulse signal and said interrupt clearing pulse signal, of the other pulse out of said interrupt setting pulse and said interrupt clearing signal; and

a delay circuit to provide, while said one pulse signal is being input to

said register, a time delay to operations of said synchronization section being operated in synchronization with said clock on which said pulse generating section used to generate said other pulse signal is operated, in order to prevent duplicated inputting of said both pulse signals to the register,
wherein each of said first and second clocks has a different clock speed and wherein said control circuit, while said interrupt setting pulse signal is being input in said register, controls said interrupt clearing pulse generating section in order to stop generation of said interrupt clearing pulse generating section by said interrupt clearing pulse generating section and wherein said delay circuit, while said interrupt setting pulse signal is outputting from the interrupt setting pulse generating section, provides a time delay to the transmission of said interrupt signal fed from said register to said first synchronization section.

18. The interrupt signal processing apparatus according to Claim 17, wherein said delay circuit is made up of a D flip-flop having a clock input terminal, data input terminal and output terminal and wherein said first clock is input to said clock input terminal and said interrupt permission signal fed from said register to said second synchronization section is input and said interrupt permission signal is output to said output terminal in synchronization with operations of said clock terminal.

19. The interrupt signal processing apparatus according to Claim 17, wherein said delay circuit is made up of an AND circuit to which an output signal fed from said register and a reversed signal of said interrupt setting pulse are input and wherein an output of said logical circuit is input to said

both synchronization sections.

20. An interrupt signal processing apparatus for processing a request for interruption from one device to the other device, connected between the one device and the other device, each being operated on either of a first clock and a second clock, comprising:

an interrupt setting pulse generating section, when receiving an interrupt requesting signal from said one device, generates an interrupt setting pulse signal by using timing provided by said first clock on which said one device is operated;

a register, when receiving said interrupt setting pulse signal, to store said interrupt setting pulse signal as a signal for interruption to said other device;

a first synchronization unit to output said interrupt signal fed from said register to the other device, in synchronization with said second clock on which the other device is operated;

an interrupt clearing pulse generating section, when receiving an interrupt clearing request signal from said other device which has received said interrupt signal through said synchronization section, to output an interrupt clearing pulse signal using timing provided by said second clock in order to reset said register used to store said interrupt signal;

a second synchronization section to output an interrupt permission signal, in synchronization with said first clock, to said one device, when said register has received said clearing pulse signal;

a control circuit provided between said interrupt setting pulse generating section and said interrupt clearing pulse generating section to

control generation, using one pulse out of said interrupt setting pulse signal and said interrupt clearing pulse signal, of the other pulse out of said interrupt setting pulse and said interrupt clearing signal; and

a delay circuit to provide, while said one pulse signal is being input to said register, a time delay to operations of said synchronization section being operated in synchronization with said clock on which said pulse generating section used to generate said other pulse signal is operated, in order to prevent duplicated inputting of said both pulse signals to the register,

wherein each of said first and second clocks has a different clock speed and wherein said control circuit, while said interrupt clearing pulse signal is being input to said register, controls said interrupt setting pulse generating section in order to stop the generation of said interrupt setting pulse signal and wherein said control circuit, while said interrupt clearing pulse signal is outputting from said interrupt clearing pulse generating section, provides a time delay to the transmission of an interrupt permission signal fed from said register to said second synchronization section.

21. The interrupt signal processing apparatus according to Claim 20, wherein said delay circuit is made up of a D flip-flop having a clock input terminal to which said second clock is input, a data input terminal to which said interrupt signal fed from said register to said first synchronization section is input and an output terminal which outputs said interrupt signal in synchronization with operations of said clock terminal and is made up of an OR circuit to which said interrupt signal fed from said output terminal of said D flip-flop and said interrupt permission signal fed from said register are input and wherein an output from said OR circuit is input to said first

synchronization section.

22. The interrupt signal processing apparatus according to Claim 20, wherein said delay circuit is made up of an OR circuit to which an output signal fed from said register and said interrupt clearing pulse are input and wherein an output from said OR circuit is input to said both synchronization sections.